**CST 133**

**Digital Electronics Design with Verilog**

**Lab 0 – Simulation tutorial**

Laboratory Objective #1: Understand how to use the ModelSim simulator to simulate digital logic circuits.

Laboratory Objective #1: Define a majority gate.

Laboratory Objective #3: Reinforce truth tables.

1. What does it mean when we say ‘majority rules’?

If a majority of the input signals are high – only two out of three in this case – then the output is high as well.

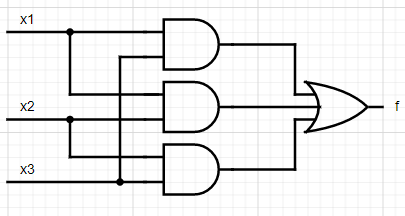
1. The majority gate is defined by the following expression.



1. Please fill out the truth table below.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| - | - | - | - | - | - | - |
| - | - | - | - | - | - | - |
| - | - | - | - | - | - | - |
| - | - | - | - | - | - | - |
| - | - | - | - | - | - | - |
| - | - | - | - | - | - | - |
| - | - | - | - | - | - | - |

1. Please provide a schematic representation of the gate (draw it out using discrete gates).

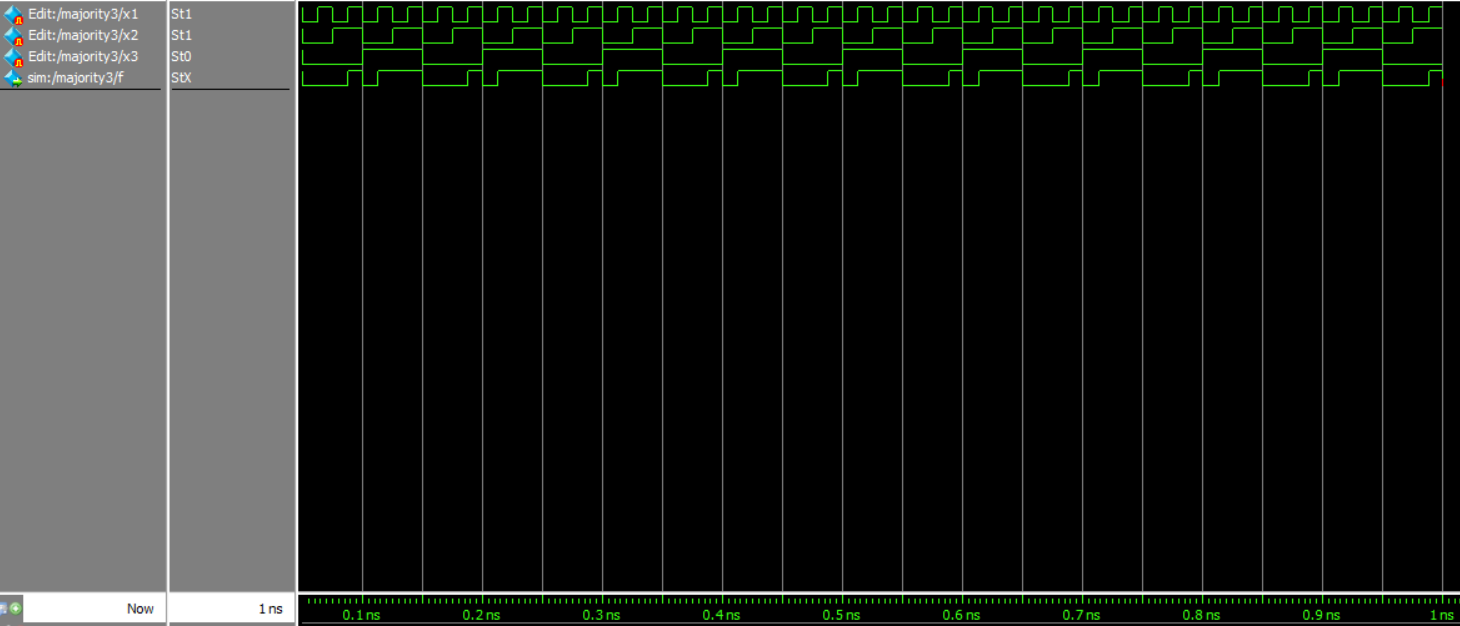


1. Okay, now follow the ModelSim tutorial here.

You might want to watch this YouTube video of how to use ModelSim before going through the Introduction. <https://www.youtube.com/watch?time_continue=220&v=jIihuC9Mxz0>

****

1. Provide a screenshot similar to Figure 30.



Submission

Submissions

The instructor does not guarantee last second availability. It is your responsibility to submit the lab in a timely manner. Note that the instructor’s mailbox may not be open after 5 PM.

A penalty of 20% per day up to 4 days will apply. After 4 days, no submissions will be accepted and you will receive a score of 0 for the lab.

For this lab you must submit the following to your instructor’s mailbox by 9 PM Pacific Standard Time on the day before your next scheduled lab.

1. This lab document completed in its entirety, with all supporting documents attached.
2. ModelSim screenshot that you created similar to Figure 30.